**EDF Implementation Report**

**Verifying the System Implementation:**

**Method 1: Analytically**

1. Calculate Hyper-period
2. CPU Load
3. Schedulability Analysis (using: A: Urm, B: Time Demand Analysis)

1. Calculate Hyper-period

Hyper-period (H)= LCM(Pi) = LCM (10 , 20 , 50 , 100) = 100

Therefore, Hyper-period = 100 ms

2. Calculate CPU Load

CPU Load (U):

U = R/C = Busy Time / (Busy Time + IDLE Time)

Note: Execution times of tasks calculated from the logic analyzer in Keil

U = ∑Ei/H = (17.7 µs\*2 +18 µs \*2+ 17.6 µs +49 µs \*5+ 5 ms \* 10 + 12 ms)/100 ms = 62.334%

3. Schedulability Analysis (using: A: Urm, B: Time Demand Analysis)

(A) Using Urm:

Urm =n (21/n – 1) = 6(21/6 – 1) = 73.477%

U = ∑ Ci/Pi = 17.7 µs / 50 ms + 18 µs / 50 ms + 17.6 µs / 100 ms + 49 µs / 20 ms + 5 ms /10 ms + 12 ms / 100 ms = 62.334%

Since U < Urm, Therefore System guaranteed Schedulable

(B) Using Time Demand Analysis:

**Method 2: Using SimSo Real-Time Scheduling Simulator**

**CPU Load**

![Table

Description automatically generated]()

![Diagram

Description automatically generated with low confidence]()**Gantt Chart**

![Graphical user interface

Description automatically generated]()**Tasks Creation**

**![Timeline

Description automatically generated]()Method 3: Using Keil**

![Table

Description automatically generated]()**CPU Load(U) = 3E =62%**

**Comment on the Results:**

As We see the results of the three methods give the same CPU load = 62%, which means a successful implementation.

**Table of Tasks**

|  |  |
| --- | --- |
| Task | Task Information |
| TICK\_HOOK | * Logic Analyzer pin: Pin 0, Port 0 |
| Button\_1\_Monitor  (Pin 0, Port 1) | * Periodicity: 50 ms * Deadline: 50 ms * Execution Time: 17.7 µs * Task Tag: 1 * Logic Analyzer pin: Pin 1, Port 0 * Priority: 1 * Button1 \_ID (ON): 1 * Button1\_ID (OFF): 2 |
| Button\_2\_Monitor (Pin 1, Port 1) | * Periodicity: 50 ms * Deadline: 50 ms * Execution Time: 18 µs * Task Tag: 2 * Logic Analyzer pin: Pin 2, Port 0 * Priority: 1 * Button2\_ID (ON): 3 * Button2\_ID (OFF): 4 |
| Periodic\_Transmitter | * Periodicity: 100 ms * Deadline: 100 ms * Execution Time: 17.6 µs * Task Tag: 3 * Logic Analyzer pin: Pin 3, Port 0 * Priority: 1 * Periodic\_String\_Available\_ID: 5 |
| UART\_Receiver | * Periodicity: 20 ms * Deadline: 20 ms * Execution Time: 49 µs * Task Tag: 4 * Logic Analyzer pin: Pin 4, Port 0 * Priority: 1 |
| Load\_1\_Simulation | * Periodicity: 10 ms * Deadline: 10 ms * Execution Time: 5 ms * Task Tag: 5 * Logic Analyzer pin: Pin 5, Port 0 * Priority: 1 |
| Load\_2\_Simulation | * Periodicity: 100 ms * Deadline: 100 ms * Execution Time: 12 * Task Tag: 6 * Logic Analyzer pin: Pin 6, Port 0 * Priority: 1 |